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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,712	04/18/2005	Philippe Gendrier	03GR029(54517)	6747

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EXAMINER	
LE, THONG QUOC	
ART UNIT	PAPER NUMBER
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,712	GENDRIER ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-100* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34,44,67,68 and 78* is/are rejected.

7)☒ Claim(s) *35,36,39-43,45-66,69,70,73-77 and 79-100* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 11/17/2006 has been entered.

2. Claims 34-100 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 34-100 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 34,44,67-68,78 are rejected under 35 U.S.C. 102(e) as being anticipated by Patelmo et al. (U.S. Patent No. 2002/0040993).

Regarding claims 34, 67-68, Patelmo et al. disclose a semiconductor memory device (Figure 1) comprising:

at least one electrically erasable and programmable non-volatile memory cell ([0002]) including

a layer of gate material (Figure 19, 60),

a floating-gate transistor (Figure 7, 28, ([0027]), including a floating gate, and further including source, drain (Figure 19, 30,49'), and channel regions defining a control gate (Figure 19, 43b, [0035], 0039),

a first active zone (Figure 1, 8, ([0021, active array 8]), and

a second active zone (Figure 1, 6 [0021, active LV6]) incorporating the control gate and electrically isolated (Figure 8, 27, 27", [0028]) from the first active zone,

a dielectric zone (Figure 19, 31, [0028, dielectric layer 31] between a first part of the layer of gate material and the first active zone (Figure 19, layer 31 between 43b and 14, label 8 in Figure 1);

the dielectric zone defining a transfer zone for transferring, during erasure of the memory cell, charges stored in the floating gate to the first active zone ([0027-0028]).

Regarding claims 44, 78, Patelmo et al. disclose wherein the floating gate transistor comprises a PMOS transistor (Figure 8, 28, [0027]).

Allowable Subject Matter

6. Claims 35-36, 69-70, 45, 39-43,46-50, 51-59, 60-66, 73-77,79-100 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Claims 35-36, 69-70, 45, 39-43,46-50, 51-59, 60-66, 73-77,79-100 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Forbes et al. (U.S. Patent No. 6,936,849), and others, does not teach the claimed invention having wherein the capacitance of the transfer zone is less than or equal to 30% of the total capacitance between the layer of the gate material and the active zones of the memory cell, and wherein the first active zone is disposed in a first substrate region having a first type of conductivity, the second active zone is disposed in a second substrate region having the first type of conductivity, the first substrate region and the second substrate region are separated by a third substrate region having a second type of conductivity, different from the first, and wherein the isolation region extends between the first substrate region and the second substrate region and includes an aperture in a contact zone in the third semiconductor region, and wherein in the erase state, the bias device causes Flower-Nordheim erasing by applying a voltage to the first active zone much higher than voltage applied to the source, drain and substrate regions of the floating gate transistor, and wherein the access transistor of a memory cell flanked by two adjacent memory cells located in a same column as the memory cell includes a first elementary access transistor specifically associated with the memory cell and second and third elementary access transistors respectively common to two access transistors assigned to the two adjacent memory cells respectively, and wherein the at least one

memory cell comprises a plurality of memory cells defining a memory plane, each memory cell including an access transistor; wherein the access transistor of a memory comprises a gate extending perpendicular to the linking part and on the opposite side from the linking part with respect to the annular gate; wherein the source of the access transistor comprises a source contact, the drain of the access transistor forms part of the source of the floating-gate transistor of the memory cell, and the drain of the floating gate transistor is electrically connected to the second active zone.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

12/27/2006